REMARKS/ARGUMENTS

The Office Action of April 25, 2008 has been carefully considered. Claims 1-13 are pending with claims 1, 7, 12 and 13 being in independent form. By the present Amendment, claims 1 and 12 have been amended to further clarify the features of the present application.

Claims 1-6 and 12 stand rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter that applicant regards as the invention. Reconsideration of this rejection is respectfully requested.

The Examiner specifically indicates that the recitation of "a circuit", "a respective circuit" and "the circuit" in claims 1 and 12 is unclear. As is noted above, claims 1 and 12 have been amended herein to further clarify the features of the present application. It is believed that claims 1 and 12, as amended herein, particularly point out and distinctly claim the features of the present application.

Claims 1, 3-7 and 9-13 have been rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Cuadra et al. U.S. 6,301,133 (hereinafter "Cuadra"). Reconsideration of this rejection is respectfully requested.

As was previously noted, the present invention relates to an ORing circuit which allows multiple power supply modules to be coupled together. Each power supply provides power to a common point. If any supply fails, power is still provided to the common point by the other supply or supplies. A circuit is coupled in series with each power supply to the common point. The circuit preferably utilizes a MOSFET transistor. The circuit is superior to conventional diode ORing circuits because the on resistance of the MOSFET is significantly lower than the typical higher forward voltage drop of a diode.

More specifically, claim 1 of the present application, for example, relates to a circuit configured for coupling a power-supplying module of a plurality of power supply modules to a common point, where one such circuit is associated with each power-supplying module of the plurality of power supplying modules to connect each power-supplying module to the common point. The circuit includes an electronically controlled transistor element configured for

conveying a current of a magnitude belonging within a predefined range, a device for detecting the direction of the current, and a control circuit configured for controlling said transistor element in such a manner that a current from the common point to one of said modules can be essentially prevented. Further, the transistor element is controlled in such a manner that a pre-selected voltage drop is produced across the transistor element independently of said current magnitude.

Cuadra discloses a plurality of power supply modules connected in parallel to a load and having associated Oring elements to selectively couple and decouple the outputs of each module to the load. Cuadra, however, does not disclose controlling the transistor element such that "a pre-selected voltage drop is produced across the transistor element independently of said current magnitude," as is required by claim 1, for example, of the present application. In contrast, in Cuadra, the MOSFET element 51 is fully saturated, that is, it is a fully enhanced FET, and thus, voltage across this element will vary in accordance with Ohm's law. That is, the voltage across the MOSFET 51 will vary with the current. While Cuadra does disclose monitoring voltage at the output terminals of the power modules, the control scheme employed in Cuadra does not separately consider the voltage drop across the transistor, but merely lumps this drop is with that of the system as a whole to maintain a constant output voltage. Thus, not only does Cuadra not disclose controlling the transistor element such that "a pre-selected voltage drop is produced across the transistor element independently of said current magnitude," as is required by claim1, there would be no advantage to doing so since Cuadra provides for output voltage regulation without this feature.

Further, Cuadra fails to disclose "a control circuit configured for controlling said transistor element in such a manner that a current from the common point to one of said modules can be essentially prevented," as is further required by claim 1, for example, of the present application. The control circuit 60 of Cuadra provides rather coarse control. That is, the control circuit 60 will not react to reverse current until that reverse current reaches a relatively high level. Specifically, as is discussed at Column 12, lines 54-58, the threshold value may be as high as 45A. Thus, substantial current is allowed to flow in the reverse direction such that Cuadra cannot be said to essentially prevent current from flowing from the common point into the modules. In contrast, the control circuit of the present application quickly prevents even very small amounts of current from flowing from the common point to the modules.

Accordingly, it is respectfully submitted that claim 1, and the claims depending therefrom, are patentable over the cited art for at least the reasons described above.

Claims 12 similarly requires "a control circuit configured for controlling said transistor element in such a manner that a current from the common point to one of said modules can be essentially prevented, further wherein said transistor element can be controlled in such a manner that a pre-selected voltage drop is produced across the transistor element independently of said current magnitude." As is noted above, Cuadra does not disclose these features.

Accordingly, it is respectfully submitted that claim 12 is patentable over the cited art for at least the reasons described above.

Similarly, claims 7 and 13 both relate to a method of coupling a number of power-supplying modules to a common point "wherein a current from the common point to said module is essentially prevented by controlling said transistor element off if a current flows from the common point to the module," and "said transistor element is controlled in such a manner that a preselected voltage drop is provided across the transistor element independently of said current magnitude." As is noted above, Cuadra does not maintain a preselected voltage drop across the transistor element independent of current magnitude and also does not prevent current from flowing from the common point to the module.

Accordingly, it is respectfully submitted that claims 7 and 13, and the claims depending therefrom, are patentable over the cited art for at least the reasons described above.

Claims 2 and 8 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Cuadra in view of Minks U.S. 4,791,349. Reconsideration of this rejection is respectfully requested.

Claims 2 and 8 depend on claims 1 and 7, respectively. As is noted above, it is believed that claims 1 and 7 are patentable over Cuadra for at least the reasons described above. Further, it is respectfully submitted that claims 1 and 7 are also patentable over Cuadra and Minks since Cuadra and Minks, either alone or in combination, fail to show or suggest the patentable features of claim 1 and 7 described above.

Accordingly, it is respectfully submitted that claims 7 and 13, and the claims depending therefrom, are patentable over the cited art for at least the reasons described above.

In view of the above, Applicant submits that all claims in this application are now in condition for allowance, prompt notification of which is requested.

Respectfully submitted,

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